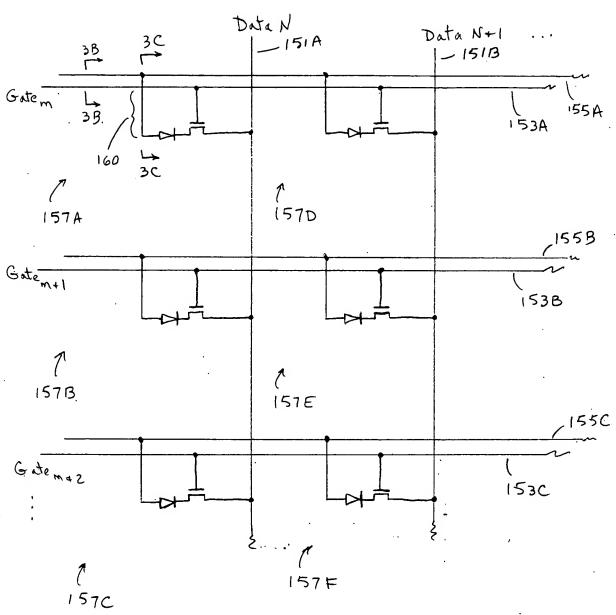
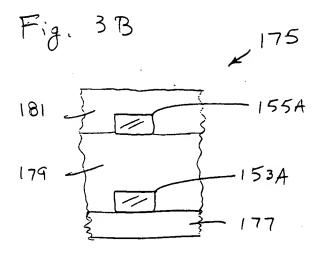


Fig. 3A × 150





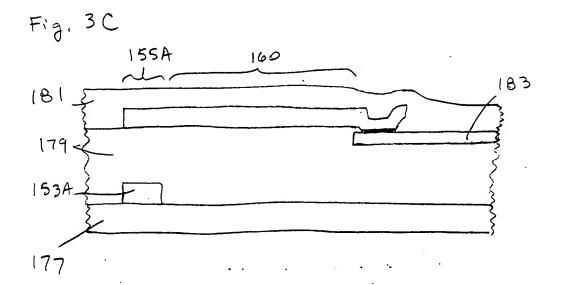
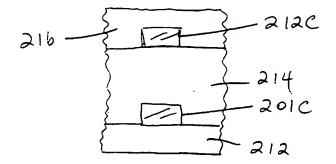
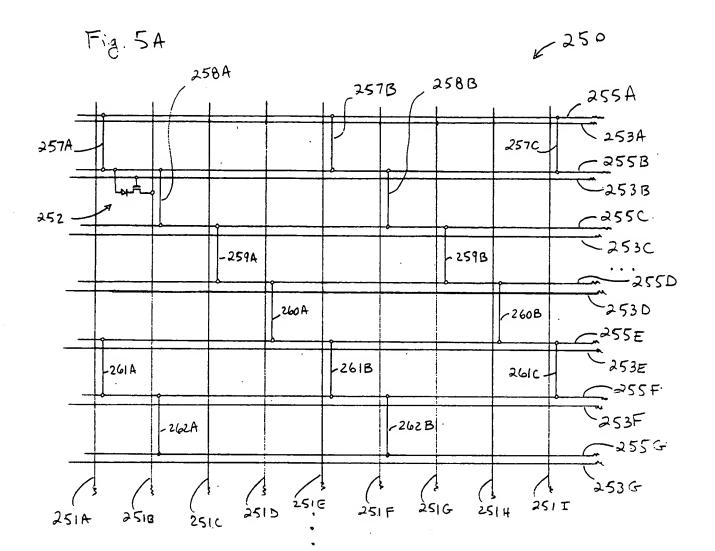
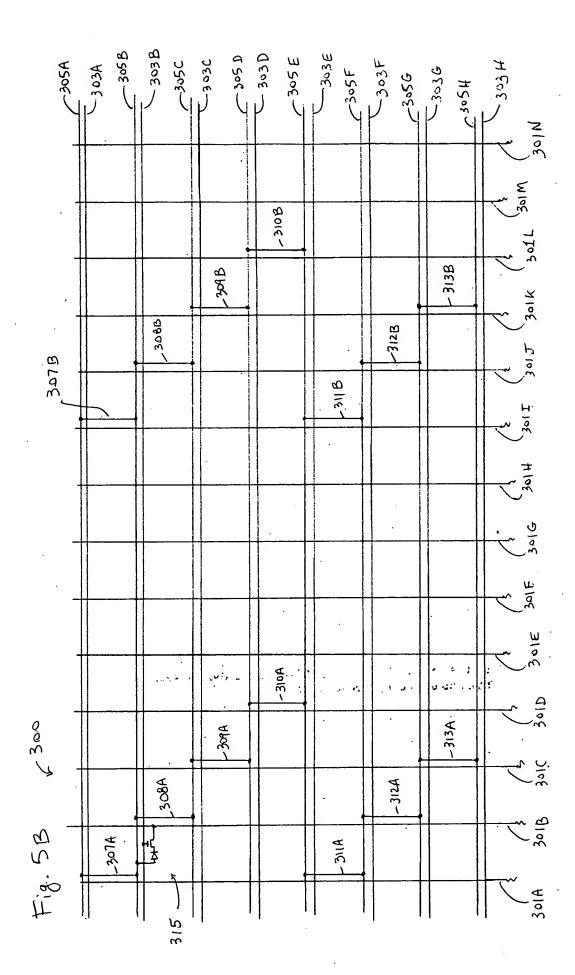


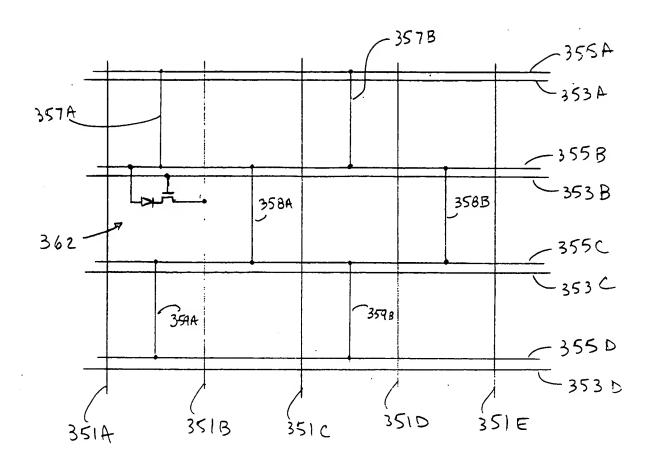
Fig. 4B



τ	Datan D	ata D	eata D	1 n+3	Dota	Data
	40					2.05A
Gate 212A	Jar.					203A
210A_	 	1 2103	1210C	1 ₂₁₀₀	↑ 210E	,205B
Gate m+1	2123-					2038
	1 210F	2106	210 H			
Gate m+2		4B	7,43			205 C m 203 C
		212	e			12050
Gate m+3						203 D
			2126			205E
Gate +4			,			203€
				2125		205F
Gate m+5						203=
				•		
	2010	/	الله الله الله الله الله الله الله الله	5	P	
		201B	2010	9010	201E	201F







The second of th

The second of the second

Form a plurality of

gate and data lines

Form a plurality

of transistors and
photodiodes

Form a mesh of bias

voltage lines with first bias

lines parallel with gate lines

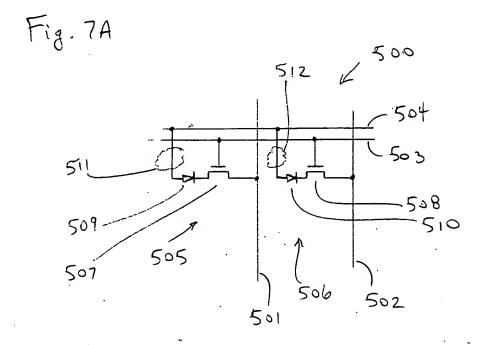
and second bias lines

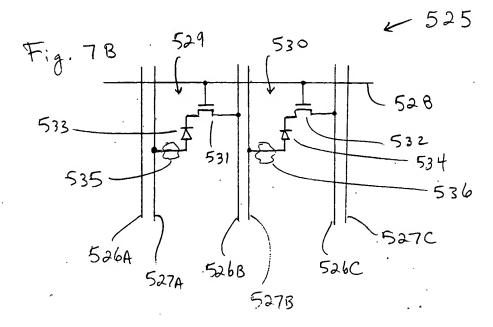
perpendicular to gate lines

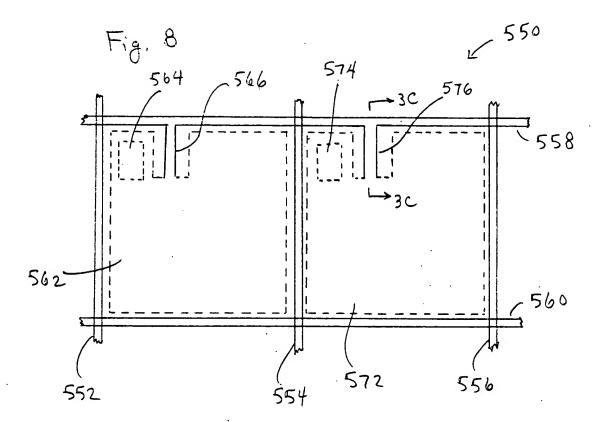
and length of first bias

lines greatly exceed length

of second bias lines







Form detecting cells with top
bias lines which include pixel
defect correcting portions which
couple bias lives to photodiodes

Test photodetector array for
defective pixels

Selectively delete defective pixels
by using pixel defect correcting
portion of defective pixel
(e.g. laser cut the bias line portion
which extends from bias line
to photodiode)